

CLAIMS

What is claimed is:

- 1 1. A method for calibrating a device, the device comprising a plurality of
2 transconductor cells, the method comprising the steps of:
3 (a) generating a test signal to the device; and
4 (b) suppressing even-order harmonics due to transistor mismatches within
5 the plurality of transconductor cells.
- 1 2. The method according to claim 1 wherein the suppressing step (b) comprises
2 the step of (b1) introducing an offset voltage on an amplifier in the plurality of transconductor
3 cells that controls the drain to source voltage of the input transistors.
- 1 3. The method of claim 2, wherein the offset voltage is controlled by a DSP in
2 order to minimize the even order harmonics upon the application of the test signal on the
3 device.
- 1 4. The method of claim 1 wherein the device comprises a second order low pass
2 filter.
- 1 5. The method of claim 1 wherein the test signal comprises a sinusoidal test
2 signal.

1 6. A calibration system comprising a device, the device including a plurality of
2 transconductor cells; and

3 a digital signal processor (DSP), the DSP for generating a test signal to the
4 device and for suppressing even order harmonics due to transistor mismatches within the
5 plurality of transconductor cells.

1 7. The system of claim 6 wherein the DSP introduces an offset voltage to each
2 amplifier in a plurality of transconductor cells that control the drain to source voltage of the
3 input transistors of the cells.

1 8. The system of claim 6 wherein the device comprises a second order low pass
2 filter.

1 9. The system of claim 7 wherein the DSP controls the offset voltage in order to
2 minimize the even order harmonics upon the application of the test signal on the device.

1 10. The system of claim 6 wherein the test signal comprises a sinusoidal test signal.